IN THE CLAIMS:

Please cancel Claims 13 and 23 without prejudice or disclaimer of subject matter, and amend the claims as shown below. The claims, as pending in the subject application, read as follows:

1. (Currently Amended) A parallel pulse signal processing apparatus, comprising:

~~including~~ a plurality of pulse output arithmetic elements;[[,]]

a plurality of connection elements which ~~parallelly~~ connect predetermined elements of the arithmetic elements in parallel;[[,]] and

a gate circuit which selectively passes pulse signals received from the plurality of connection elements,

~~characterized in that said~~ wherein the pulse output arithmetic elements comprise; ~~comprises~~

input means for inputting a plurality of time series pulse signals;[[,]]

modulation processing means for executing predetermined modulation processing on [[the]] a basis of the input plurality of time series pulse signals ~~which are input~~;[[,]] and

pulse output means for outputting a pulse signal on [[the]] a basis of a result of the modulation processing, and

wherein said gate circuit ~~selectively passes~~ counts, of the pulse signals output from the plurality of pulse output arithmetic elements and received from said plurality of connection elements, ~~a finite number of~~ pulse signals corresponding to

predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number.

2. (Currently Amended) The apparatus according to claim 1, ~~characterized by~~ further comprising a timing signal generation circuit to generate a predetermined timing signal,

wherein after the predetermined timing signal from said timing signal generation circuit is input to said gate circuit, said gate circuit ~~selectively passes~~ counts, of the pulse signals output from the plurality of pulse output arithmetic elements and received from said plurality of connection elements, the ~~finite number of~~ pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until the number of the counted pulse signals reaches the predetermined number.

3. (Currently Amended) The apparatus according to claim 2, ~~characterized in that~~ wherein said gate circuit ~~selectively passes~~ counts, of the pulse signals output from the plurality of pulse output arithmetic elements and received from said plurality of connection elements, the pulse signals in ascending order of delays with respect to the timing signal from said timing signal generation circuit, and passes the pulse signals corresponding to the predetermined upper output levels until the number of the counted pulse signals reaches the predetermined number.

4. (Currently Amended) The apparatus according to claim 1, wherein ~~characterized in that~~ said gate circuit is arranged on ~~connected to~~ a predetermined bus connected to said plurality of connection elements and ~~selectively~~ passes the predetermined ~~finite~~ number of pulse signals corresponding to the predetermined upper output levels from among the pulse ~~signal~~ signals propagating on the bus.

5. (Currently Amended) The apparatus according to claim 1, wherein ~~characterized in that~~ said arithmetic element integrates an input pulse signal train in a predetermined time window and outputs the pulse signal at one of a phase and a frequency corresponding to [[the]] an integration value.

6. (Currently Amended) The apparatus according to claim 1, wherein ~~characterized in that~~ said gate circuit includes a switching circuit selectively connected to, of said plurality of connection elements, a connection element whose connection strength takes a maximum value and not less than a predetermined level.

7.(Currently Amended) A parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations, ~~characterized by~~ comprising:

a plurality of arithmetic elements which ~~receive~~ receives signals from different layer levels and outputs predetermined pulse signals by a predetermined local receptor field structure; and

a gate circuit element which ~~selectively passes~~ counts, of the pulse signals output from said plurality of arithmetic elements belonging to a predetermined receptor field, pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number ~~in accordance with a signal level of the pulse signal~~.

8. (Currently Amended) A parallel pulse signal processing apparatus comprising: ~~including~~

input means for inputting data in a predetermined dimension;[[,]]

a plurality of data processing means;[[,]]

a gate circuit which selectively passes pulse signals from said data processing means;[[,]] and

output means for outputting a result of pattern detection,

~~characterized in that~~ wherein said data processing means includes a plurality of arithmetic elements ~~parallelly~~ connected by predetermined connection means in parallel,

wherein said arithmetic elements included in said data processing means ~~outputs~~ output a pulse shaped signal train representing a detection result of a pattern of a predetermined category on [[the]] a basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined time window, [[and]]

wherein said gate circuit counts, of pulse signals included in the pulse shaped signal train output from the plurality of arithmetic elements and received from said plurality of connection elements, pulse signals corresponding to predetermined upper

output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number, and

wherein said output means outputs the detection result of the predetermined pattern in the data on [[the]] a basis of the outputs from said arithmetic elements.

9. (Currently Amended) A parallel pulse signal processing apparatus comprising; ~~including~~

input means for inputting data in a predetermined dimension;[[,]]

a plurality of data processing means for outputting pulse signals;[[,]]

a gate circuit which selectively passes pulse signals output and received from said data processing means;[[,]] and

output means for outputting a result of pattern detection,

~~characterized in that~~ wherein said data processing means includes a plurality of arithmetic elements ~~parallelly~~ connected by predetermined connection means in parallel,

wherein said gate circuit counts, ~~selectively passes the pulse signals on the basis of signal levels~~ of the pulse signals output and received from said plurality of data processing means, pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number,

wherein said arithmetic elements receive a time series pulse signal, identify time series pulse signal patterns of a plurality of classes, and output a pulse shaped signal train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window, and

wherein said output means outputs the detection result of [[the]] a predetermined pattern in the data on the basis of the outputs from said arithmetic elements.

10. (Currently Amended) A parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations, ~~characterized by~~ comprising:

input means for inputting one of an intermediate result of different layer levels and data from a predetermined memory;

a plurality of data processing means, having a feature detection layer which detects a plurality of features from the data input by said input means, for outputting pulse signals; and

a timing signal generation circuit,

wherein said plurality of data processing means further comprises: ~~comprising~~

a plurality of arithmetic elements which receives detection signals of the features of different types from a layer level of a preceding stage and outputs predetermined pulse signals;[[,]] and

a gate circuit which ~~selectively passes outputs~~ counts, of the pulse signals output from said arithmetic elements involved in the plurality of predetermined features, pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number, and

wherein said arithmetic elements output the pulse ~~shaped~~ signals at one of a frequency and a timing based on a plurality of input signals from said timing signal generation circuit and an arrival time pattern of a plurality of pulses in a predetermined time window.

11. (Currently Amended) The apparatus according to claim 1, wherein ~~characterized in that~~ said gate circuit includes a switching circuit selectively connected to, of said plurality of connection elements, a connection element whose connection strength [[has]] is not less than a predetermined level.

12. (Currently Amended) The apparatus according to claim 1, wherein ~~characterized in that~~ said gate circuit counts ~~selectively passes~~, of the pulse signals output from the plurality of pulse output arithmetic elements and received from said plurality of connection elements, the pulse signals in ascending order of delays with respect to a predetermined reference time, and passes the pulse signals corresponding to the predetermined upper output levels until the number of the counted pulse signals reaches the predetermined number.

13. (Cancelled)

14. (Currently Amended) The apparatus according to claim 1, wherein ~~characterized in that~~ said gate circuit counts ~~selectively passes~~, of the pulse signals output from the plurality of pulse output arithmetic elements and received from said plurality of

connection elements, ~~a predetermined number of~~ pulse signals having a local maximum value from an uppermost level, and passes the signals having the local maximum value until a number of the counted pulse signals reaches a predetermined number.

15. (Currently Amended) The apparatus according to claim 7, wherein ~~characterized in that~~ said gate circuit counts ~~selectively passes~~ pulse signals corresponding to upper output levels, and passes the pulse signals corresponding to the upper output levels until a number of the counted pulse signals reaches a predetermined number, for each feature.

16. (Currently Amended) A pattern recognition apparatus ~~characterized by~~ comprising a parallel pulse signal processing apparatus of claim 1.

17. (Currently Amended) An image input apparatus, wherein ~~characterized in that~~ pattern recognition is executed by using a parallel pulse signal processing apparatus of claim 1, and input control of a predetermined image signal is executed on [[the]] a basis of [[the]] a pattern recognition result.

18. (Currently Amended) A control method of a parallel pulse signal processing apparatus, said apparatus including ~~comprising~~ a plurality of pulse output arithmetic elements, a plurality of connection elements which ~~parallelly~~ connect predetermined arithmetic elements in parallel, and a gate circuit which selectively passes

pulse signals received from the plurality of connection elements, wherein said control method comprises:

using the arithmetic elements to perform:

~~characterized in that the arithmetic element inputs~~ inputting a plurality of time series pulse signals;[[,]]

~~executes~~ executing predetermined modulation processing on the basis of the input plurality of time series pulse signals ~~which are input~~;[[,]] and

~~outputs~~ outputting a pulse signal on [[the]] a basis of a result of the modulation processing, and

wherein the gate circuit ~~selectively passes~~ counts, of the pulse signals output from the plurality of pulse output arithmetic elements and received from said plurality of connection elements, ~~a finite number of~~ pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number.

19. (Currently Amended) A control method of a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations, ~~characterized by~~ comprising:

~~causing~~ receiving by a plurality of arithmetic elements ~~to receive~~ signals from different layer levels and ~~output~~ outputting by the plurality of arithmetic elements predetermined pulse signals by a predetermined local receptor field structure; and

~~causing~~ counting by a gate circuit element, of ~~to selectively pass~~ the pulse signals output from the plurality of arithmetic elements belonging to a predetermined

receptor field, pulse signals corresponding to predetermined upper output levels and passing by the gate circuit element the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number ~~in accordance with a signal level of the pulse signal~~.

20. (Currently Amended) A control method of a parallel pulse signal processing apparatus, said apparatus including ~~comprising~~ input means for inputting data in a predetermined dimension, a plurality of data processing means, a gate circuit which selectively passes signals from the data processing means, and output means for outputting a result of pattern detection, wherein said control method comprises:

~~characterized by comprising causing~~ outputting by each of a plurality of arithmetic elements, which are included in the data processing means and ~~parallelly~~ are connected by predetermined connection means in parallel, ~~to output~~ a pulse shaped signal train representing a detection result of a pattern of a predetermined category on [[the]] a basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined time window;[[, and]]

counting by the gate circuit, of pulse signals included in the pulse shaped signal train output from the plurality of arithmetic elements and received from said plurality of connection elements, pulse signals corresponding to predetermined upper output levels, and passing by the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number; and

~~causing~~ outputting by the output means ~~to output~~ the detection result of the predetermined pattern in the data on [[the]] a basis of the outputs from the arithmetic elements.

21. (Currently Amended) A control method of a parallel pulse signal processing apparatus, said apparatus including ~~comprising~~ input means for inputting data in a predetermined dimension, a plurality of data processing means for outputting pulse signals, a gate circuit which selectively passes pulse signals output and received from the data processing means, and output means for outputting a result of pattern detection, wherein said control method comprises:

~~characterized by comprising causing~~ counting by the gate circuit, ~~to selectively pass the pulse signals the basis of signal levels~~ of the pulse signals output and received from said plurality of data processing means, pulse signals corresponding to predetermined upper output levels, and passing by the gate circuit the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number;[[,]]

~~causing~~ receiving by a plurality of arithmetic elements, which are included in the data processing means and ~~parallelly~~ are connected by predetermined connection means in parallel, ~~to receive~~ a time series pulse signal, ~~identify~~ identifying time series pulse signal patterns of a plurality of classes, and ~~output~~ outputting a pulse shaped signal train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window;[[,]] and

~~causing~~ outputting by the output means ~~to output~~ the detection result of [[the]] a predetermined pattern in the data on [[the]] a basis of the outputs from the arithmetic elements.

22. (Currently Amended) A control method of a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations, the parallel pulse signal processing apparatus ~~comprising~~ including input means for inputting one of an intermediate result of different layer levels and data from a predetermined memory, a plurality of data processing means, having a feature detection layer which detects a plurality of features from the data input by the input means, for outputting pulse signals, and a timing signal generation circuit, wherein said control method comprises:

~~characterized by comprising,~~ under the control of the data processing means, ~~causing~~ receiving by a plurality of arithmetic elements ~~to receive~~ detection signals of the features of different types from a layer level of a preceding stage and output predetermined pulse signals;[[, and]]

~~causing~~ counting by a gate circuit element, of the pulse signals ~~to selectively pass outputs~~ output from the arithmetic elements involved in the plurality of predetermined features, pulse signals corresponding to predetermined upper output levels, and passing by the gate circuit element the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number;[[,]] and

~~causing~~ outputting by the arithmetic elements ~~to output~~ pulse shaped signals at one of a frequency and a timing based on a plurality of input signals from the timing

signal generation circuit and an arrival time pattern of a plurality of pulses in a predetermined time window.

23. (Cancelled)

24. (Currently Amended) A control method of an image input apparatus ~~characterized by~~ comprising executing pattern recognition by using a parallel pulse signal processing apparatus of claim 1, and executing input control of a predetermined image signal on [[the]] a basis of [[the]] a pattern recognition result.